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EXAMINER
MCLEAN MAYO, KIMBERLY N

ART UNIT	PAPER NUMBER
2187	4

DATE MAILED: 07/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/991,128	KAHN ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Information Disclosure Statement submitted on February 27, 2002 and the Application submitted on November 14, 2001.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 16 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 16 and 21 depend from claims 10, [via claim 15] and claim 17 [via claim 20], wherein claims 10 and 17 state that the first data is changeable and the second data is not changeable after the circuit is reset and initialized and thus how can the first data also be unchangeable after initialization with respect to claim 16 and how can the second data also be changeable after initialization with respect to claim 21. Clarification is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-7, 9-10, 12-15, 17-20, 22-28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Schell et al. (USPN: 6,314,520).

Regarding claims 1, 3 and 5, Schell discloses a circuit [memory controller] comprising a first control register (Figure 3, Reference 96 within Reference 14 in Figure 1; RCV mask and offset register) to be loadable after the circuit is reset (C 5, L 2-5); a first plurality of control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again (Figure 3, References 68, 90 and 92 within Reference 14 in Figure 1; C 4, L 17-26, L 59-67; C 5, L 1-2; C 6, L 15-18); and a first switch unit (software/internal logic within Reference 20 in Figure 3 within Reference 14 in Figure 1 which controls outputting data to comparators 74 and 100 in Figure 3 within Reference 14 in Figure 1) coupled to the first control register and the first plurality of control registers, wherein the first switch unit outputs data [to Reference 100 in Figure 3] stored by one control register of the first plurality of control registers as a function of the data loaded in the first control register (C 5, L 5-25).

Regarding claims 4, 13-14 and 19, Schell discloses the software control causing the first register to be loaded with different data in response to a change in the circuit's operational mode, which is user-selectable via the network, wherein the network is the user (an operation mode change occurs when a different packet is sent to Reference 96 in Figure 3)(C 5, L 2-5).

Regarding claims 6-7, 15 and 20, Schell discloses the first plurality of control registers loaded by a BIOS during an initialization process after the circuit is reset (C 4, L 17-26, L 59-67; C 5, L 1-

2 - initialization intrinsically occurs after a reset) and locked by the BIOS during the initialization process after the circuit is reset (C 5, L 52-58).

Regarding claim 9, Schell discloses a second control register (Figure 3, Reference 96 within Reference 15 in Figure 1; RCV mask and offset register) to be loadable after the circuit is reset (C 6, L 15-18 – initialization intrinsically occurs after a reset); a second plurality of control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again (Figure 3, References 68, 90 and 92 within Reference 15 in Figure 1; C 4, L 17-26, L 59-67; C 5, L 1-2); and a second switch unit (software/internal logic within Reference 20 in Figure 3 with Reference 15 in Figure 1 which controls outputting data to comparators 74 and 100 in Figure 3 within Reference 15 in Figure 1) coupled to the second control register and the second plurality of control registers, wherein the second switch unit outputs data [to Reference 100 in Figure 3] stored by one control register of the second plurality of control registers as a function of the data loaded in the second control register (C 5, L 5-25).

Regarding claims 10, 12 and 17-18, Schell discloses means for storing first data (data stored in Reference 96 in Figure 3) and second data, the second data including a plurality of portions (portions comprised of data stored in References 68, 90 and 92 in Figure 3) (C 5, L 2-5, C 4, L 17-26, L 59-67; C 5, L 1-2; C 6, L 15-18) wherein after the circuit is reset and initialized the first data is changeable and the second data is not changeable (the second data is stored in locked registers [refer to C 5, L 52-58] and the first data is not stored in locked registers and thus there

is no disclosed means for preventing a write to the first data and thus the first data is changeable); and means (software/internal logic within Reference 20 in Figure 3 which controls outputting data to comparators 74 and 100 in Figure 3) for selecting one portion of the plurality of portions in response to the first data, wherein the selected portion is provided to another unit of the circuit (Reference 100 in Figure 3) (C 5, L 5-25).

Regarding claims 22-27, Schell discloses loading a plurality of controls registers of a circuit, the plurality of control registers including a plurality of protected registers (Figure 3, References 68, 90 and 92) and unprotected registers (Figure 3, References 84, 85 and RCV mask and offset register within Reference 96 in Figure 3) (C 5, L 2-5, C 4, L 17-26, L 59-67; C 5, L 1-2; C 6, L 15-18); locking the plurality of protected control registers (C 5, L 52-58); selecting a locked control register of the plurality of control registers as a function of data stored in an unprotected control register of the plurality of control registers and outputting [to Reference 100 in Figure 3] data stored by the selected locked control register (C 5, L 5-25); deselecting the locked control register and selecting another locked control register of the plurality of protected control registers (when the software/internal logic within Reference 20 in Figure 3 which controls outputting data to comparators 74 and 100 in Figure 3, switches to outputting data to Reference 74, the register output to Reference 100 is effectively deselected)(C 4, L 30-46).

Regarding claims 28 and 30, Schell discloses a processor (Figure 2, Reference 26); a memory (memory within Reference 12 in Figure 1); and a memory controller (Reference 20 in Figure 2) coupled to the processor and the memory [via Reference 18], the memory controller comprising

a first control register (Figure 3, Reference 96 in Figure 3; RCV mask and offset register) to be loadable after the circuit is reset (C 5, L 2-5); a first plurality of control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again (Figure 3, References 68, 90 and 92; C 4, L 17-26, L 59-67; C 5, L 1-2; C 6, L 15-18); and a first switch unit (software/internal logic within Reference 20 in Figure 3 which controls outputting data to comparators 74 and 100 in Figure 3) coupled to the first control register and the first plurality of control registers, wherein the first switch unit outputs data [to Reference 100 in Figure 3] stored by one control register of the first plurality of control registers as a function of the data loaded in the first control register (C 5, L 5-25).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 11 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schell (USPN: 6,314,520) in view of Circello (PGPUB: US 2003/0061461).

Schell discloses the limitations cited above in claims 1, 10 and 28, however, Schell does not disclose the switch unit comprising a multiplexer having input ports coupled to receive output from the first plurality of control registers and having a control port coupled to receive output from the first control register. Circello teaches the concept of a switch unit comprising a

multiplexer (Figure 2, Reference 68) having input ports coupled to receive output from the first plurality of control registers (Figure 2, References 70-72) and having a control port coupled to receive output from the first control register (the control port of Reference 68 receives an address output {refer to 2[19:18] coupled to Reference 68} from an address register within Reference 28 in Figure 1, which outputs an address to Reference 40 in Figure 2). These features taught by Circello provide flexibility to the system by allowing the system to operate with different addressing modes which are implemented using the above features. Thus, it would have been obvious to one of ordinary skill in the art to use Circello's teachings with the teachings of Schell for the desirable purpose of flexibility.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schell (USPN: 6,314,520) in view of Rapp (PGPUB: US 2001/0014036).

Schell discloses the limitations cited above, however, Schell does not disclose the plurality of control registers including a lock bit to set by the BIOS to lock the plurality of control registers during the initialization process after the circuit is reset. However, Rapp teaches the concept of including a plurality of memory locations [register storage units] with a lock bit lock the corresponding memory location (Page 1, Section [0004]). This feature taught by Rapp provides a simple and efficient means for locking storage locations. Schell does not explicitly disclose how the lock functionality is the system is performed, however, one of ordinary skill in the art would have recognized the simple design and efficiency afforded by the Rapp's teachings and accordingly would have been motivated to use Rapp's teachings with Schell's system for the desirable purpose of simpler design and efficiency.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

DeRoo – USPN: 5,623,673 – write once registers.

Gephardt – USPN: 5,623,673 – lock register which not changeable in normal mode.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

June 26, 2003